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Title: A Continuous-Time Multi-Gigahertz Filter using Transmission Line Delay Elements

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Front Page View: FIG. 2

References:

U.S Patent Documents

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Other References

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3. Castello et. al., "Performance Limitations in Switched-Capacitor Filters, "IEEE Transactions on Circuits and Systems, vol. CAS-32, no. 9, pp. 865-876, Sept. 1985.

4. Martin et. al., "Effects of the Op Amp Finite Gain and Bandwidth on the Performance of Switched-Capacitor Filters," IEEE Transactions on Circuits and Systems, vol. CAS-28, no. 8, pp. 822-829, Aug. 1981.
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Background - Technical Field of Invention

This present invention relates to analog implementations of finite impulse response (FIR) filters and infinite impulse response (IIR) filters. The filter application examples include but are not limited to equalization of 10Gb/s and 40Gb/s fiber optic transmission systems, multi-gigahertz serial chip-to-chip communications, multi-gigahertz serial backplane communications, high-speed network communications, disk drive channel equalization, and filtering for radio frequency (RF) systems. Additionally, the FIR and IIR filter coefficients can be programmed so as to form an adaptive equalizer.

Background of the Invention and Discussion of Prior Art

A FIR or IIR filter is a basic building block of digital filtering systems. Typically for low frequency filtering (less than 100 MHz), as in modems, FIR or IIR filtering can be done with a DSP processor or ASIC using CMOS digital logic. At higher speeds, between 10 MHz

and 1 GHz, a digital filtering solution will dissipate very high power and requires large die area, and a CMOS analog solution becomes attractive in order to reduce power and area. However, at speeds of 1 GHz and above, both digital and analog solutions become problematic even in higher speed technologies such as SiGe, InP, and GaAs.

A block diagram of a typical FIR filter structure is shown in Figure 1. The FIR filter consists of delay line elements, **1, 2, and 3**, coefficients **A, B, C, and D**, coefficient multipliers, **4, 5, 6, and 7**, and a summing circuit, **8**. The input, **X1**, is successively passed through the fixed delay elements, **1, 2, and 3**. The signals at the successful nodes of the delay elements **1, 2,** and **3** are then multiplied by coefficients **A, B, C, and D**, respectively, before being summed to produce the output, **Y1**. Prior art analog implementations of FIR filters have been published in the literature using switched-capacitor filtering to implement delay elements, multipliers, and summers. Unfortunately, switched-capacitor circuits are limited in speed by the gain-bandwidth product of the operation amplifiers, which is limited by the speed of the technology. Higher gain gives better linearity performance, yet requires the speed to be reduced. Hence, there is also a severe speed versus linearity tradeoff in traditional designs. Other methods for implementing these types of filters exist, but all share high frequency performance limitations.

Objects and Advantages of the Invention

Accordingly, it is a primary object of the present invention to provide an analog FIR and IIR filter implementation that improves upon the speed of current implementations into the hundreds of gigahertz range with superior linearity to the implementations of the prior art.

Summary of the Invention

The present invention achieves the above objectives and advantages by taking advantage of the properties of transmission lines. A transmission line provides a fixed impedance value over a wide range of frequencies with excellent linearity. This easily includes ranges up to and exceeding 100 GHz. In addition, the propagation delay of signals propagating down a transmission line can be precisely controlled only by the dimensions of the transmission line and the physical properties of the medium in which the transmission line is built. The inventor notes that these properties of the transmission line make it an ideal element for the delay stages of the FIR filter and are not subject to the linearity/bandwidth limitations of active delay stages.

Description of Drawings

Figure 1 is a block diagram of a 4-tap FIR filter considered as prior art.

Figure 2 is a block diagram of a 4-tap analog FIR filter constructed with the principles of the invention.

Figure 3 is a block diagram of a 1-tap analog IIR filter constructed with the principles of the invention.

Description of the Preferred Embodiment

Taking advantage of these transmission line properties, the preferred embodiment of the high speed analog FIR filter is shown in Figure 2. The input voltage, **X2**, enters a transmission line of segments with each segment providing its own fixed propagation delay to implement the delay elements, **10, 11, and 12,** while each of the analog transconductance elements, **13, 14, 15** and **16** with its own transducer factor Gm is used as a coefficient multiplier to convert the input voltage to a current. The outputs of the analog transconductance elements, **13, 14, 15,** and **16** are connected together, causing the currents to be summed at the input of the impedance or transimpedance element, **17.** The transimpedance element, **17,** converts its input current back to a voltage at **Y2**. The transimpedance element, **17,** can also be implemented as a transimpedance amplifier with the same functionality. The transconductance element is typically implemented as an amplifier that is subject to the gain-bandwidth tradeoffs as in the prior art, however, the delay elements are not. In this way, the total bandwidth of the FIR filter circuit can be significantly extended compared to the prior art, and the linearity performance can be improved. The value of the coefficient taps can be controlled by modifying the transconductance, or Gm, of the analog amplifiers. The values of Gm can be fixed, programmable, or adaptively controlled. The transmission line is terminated at the end with impedance element, **18.** The termination impedance, **18,** can be matched to the transmission line characteristic impedance in order to

eliminate reflections, or can be purposely mismatched to induce a reflection that will alter the response of the filter.

The same building blocks used in the FIR filter circuit of Figure 2 can be used to create an infinite impulse response (IIR) filter as shown in Figure 3. An IIR filter uses feedback in its filter structure. The voltage input, **X3**, is multiplied by a coefficient and converted to a current using transconductance element, **20**. The voltage output, **Y3**, is multiplied by a coefficient and converted to a current using transconductance element, **21**. The resultant currents are summed at the input of transimpedance or impedance element, **22**, which converts the summed currents at its input into a voltage at its output, node **E**. The voltage at node **E** delayed with transmission line based delay element, **23**, whose output is the output of the filter, **Y3**. As in the FIR filter, the transconductance elements can be implemented as transconductance amplifiers, and the multiplying coefficients can be controlled by modifying the transconductance, Gm, of the analog amplifiers. The values of Gm can be fixed, programmable, or adaptively controlled. As in the FIR, the transmission line is terminated with an impedance element, **24**. The termination impedance, **24**, can be matched to the transmission line characteristic impedance in order to eliminate reflections, or can be purposely mismatched to induce a reflection that will alter the response of the filter.

Those skilled in the art will recognize that certain modifications to the intended patent are intended to be within the scope of this patent. These include additional components added to the inputs of the transconductance amplifiers to improve input matching. Those skilled in the art will also recognize that the invention does not depend on the type of transmission line, or if it is implemented on the chip substrate, the package substrate, or the printed circuit board. Those skilled in the art will also recognize that there are many variations of transconductance and transimpedance amplifiers, and that there can be multiple stages of amplification and conversions between voltage and current that are intended to be within the scope of this patent. Those skilled in the art will recognize that other embodiments that utilize the transmission line as a delay element in their filters, including finite impulse response (FIR) or infinite impulse response (IIR) filters, or feed-forward equalization (FFE) filters or decision feedback equalization (DFE) filters, are intended to be within the scope of this patent. These and other modifications, which are obvious to those skilled in the art, are intended to be included within the scope of the present invention. Accordingly, the scope of the invention should be determined not by the embodiment described, but by the appended claims and their legal equivalents.